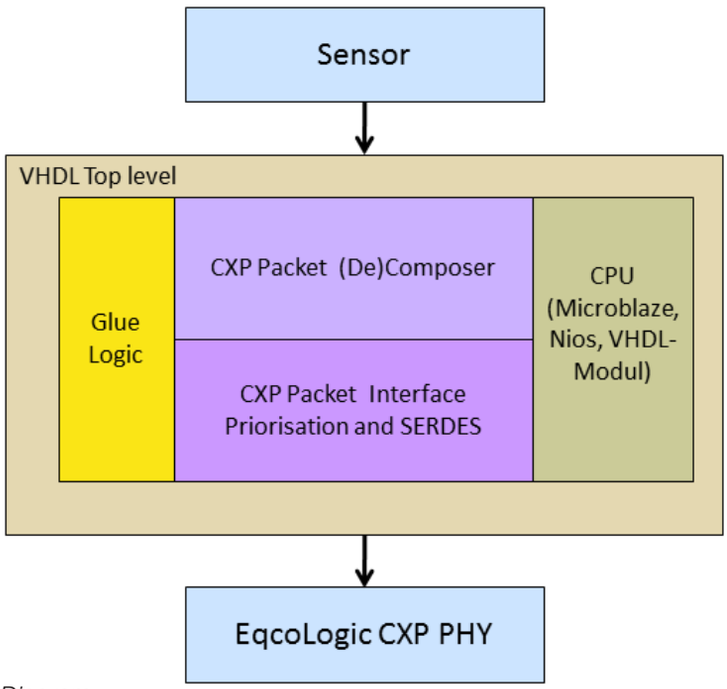
sensor to image

CoaXPress – FPGA Core

CoaXPress® – compliant IP Core for FPGAs

CoaXPress® is a standardized communication protocol for vision applications based on the widely used RG59 coaxial cables, which are used for PAL/NTSC video as well. It allows easy interfacing between cameras and frame grabbers, because the protocol is well defined and supports GeniCam™ software standard.

Sensor to Image offers a set of IP cores and a development frame-work to build FPGA-based products with CoaXPress inter-face.



Block Diagram CXP Design

Due to the speed of CoaXPress, a sender as a receiver needs a fast implementation in a FPGA with preferable embedded SERDES inside the FPGA. These SERDES are available up from Spartan 6 T devices or Cyclone IV GX devices. Our core is small enough that it leaves enough space for your application even using the smallest device out of these families.

The CXP FPGA solution is delivered as a reference design with FPGA IP cores, which allows a maximum in performance at a small footprint and enough flexibility to realize your custom solutions.

The following components are part of the design:

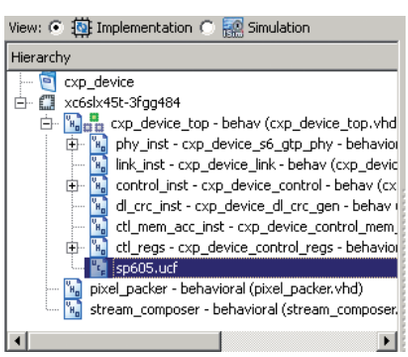
Top Level Design, which builds the interface between real hardware (e.g. sensor, CPU, CXP physical) and internal data processing. This module is delivered in source-code (VHDL), so it can be adapted and extended to custom hardware.

The CXP Streaming Interface takes all data from the video sensor output to the CXP PHY. It realizes the full speed on Streaming Channel according to the CXP-specification.

The CXP Control Interface receives and sends all data from CXP controll channel from and to the CXP PHY and realizes the control channel according to the CXP-specification.

An FPGA integrated CPU (MicroBlaze or NIOS) is used for several non time critical control and configuration tasks on the CXP-RX as -TX core and can be replaced by the user in a VHDL state machine to save FPGA space in the final application.

Some software parts are delivered as compiled files only (e.g. CXP-bootloader, CXP-controller), other parts are in source code. The delivered design framework comes with all necessary design files and cores, ISE, VIVADO or QUARTUS project files and a CXP camera system with a CMOS imager. This system should be used as reference design and evaluation board. As development environment the XILINX or ALTERA development tools are used (not in scope of delivery).



ISE Project Tree

Available Modules

Module	Comment	ALTERA FPGA	XILINX FPGA
Sync. bus as sensor interface	incl. 1 single tap sensor adaption incl. I²C/SPI core + C code	•	•
CXP Core project licence	packet composer, PHY interface	•	•
XML-File generation	XML-File generation	•	•
Full sources, design, …	on request	•	•

other FPGA vendors on request

CXP Device Resources (1 Lane)

Module	Artix-7	Kintex-7	Arria V GX	Cyclone IV
CXP Device Core				
– Slice registers	3134	3078	3578	3310
– Slice lookup tables	3161	2948	2511	3841
– Block RAMs	7	6	18	8
– Maximum clock frequency	202 MHz	298 MHz	208 MHz	246 MHz
CXP transport layer				
– Transceiver	1	1	1	External SERDES
– clock Manager	1	1	1	1
– Maximum Link speed	6.25 Gbit	6.25 Gbit	6.25 Gbit	2,5Gbit

values are post synthesize only and based on platform specific reference designs, other architectures might have different resource usage

CXP Host Resources (4 Lane)

Module	Artix-7	Kintex-7	Arria VGX	Cyclone IV
CXP Decomposer Host Core				
– Slice registers	4445	4558	15290	N/A
– Slice lookup tables	5486	5357	9175	–
– Block RAMs	17	17	49	–
– Maximum clock frequency	265 MHz	280 MHz	256 MHz	–
CXP Transport layer				
– Transceiver	4	4	4	–
– clock Manager	1	1	1	–
– Maximum Link speed	6.25 Gbit	6.25 Gbit	6.25 Gbit	–

CXP FMC DEVICE Evaluation Board

TECHNOLOGY

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